Optimizing Power IC Layouts by Simulation Tools

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***Abstract*— Power Integrated Circuit (IC) needs to consume huge currents so it often includes a large size device. In order to approach IC driving capabilities, 1.5 times to the simulation size can be used. In this study, 40 % reduction in IC layout can be reached after the correct simulation tool flow is adopted.**

I. Introduction

Large Array Device (LAD) is often applied for the consumer electronic integrated circuits' driving capabilities [1]. The ratio of LAD layout area to one pure power IC area can be from 20% to 70% so LAD layout is a frequent discussion topic. Many layout related papers are published [2-5]. They are about waffle type layouts, pre-layout estimations, fully automatic layout optimization and layout considerations in power amplifiers. They are very important, but there is no big layout area saving in those discussions.

This paper research is implemented by one simple simulation tool which majorly provides turn-on resistances and current density distributions (not discussed in this study). Adding the simulation at the 1st design stage can save a lot of layout areas, but still there are good IC performances. Different device types, sizes, measurements and bonding types are analyzed by processed in Bipolar CMOS DMOS (BCD) and Silicon on insulator (SOI).

For one IC design, silicon driving capability can be a major concern. In order to meet the driving target, circuit designers can use the larger layout size than that from Spice simulation. Of course, there is another kind of post-layout simulation tool which can extract the resistance and capacitance for evaluating the required size more precisely, but the post-layout simulation tool is very expensive and time consuming. In this study, we try to use the simple and quick simulation tool R3D (SILICON FRONTLINE tool; Taiwan agent: Kaviaz) for evaluating the device size.

II. SOI Data Results and Analyses

For simulations, there are two resistance data from the simulation tool R3D. They are device channel resistance Rch1 from Simulation Program with Integrated Circuit Emphasis (Spice) model and interconnect resistance Rm1 from tool R3D simulations, based on the process interconnect data. Tool R3D combines both Spice front-end resistances and back-end process metal routing resistances for evaluating device's total resistances. For measurements, there are two kinds of data obtained from HP4156, w/o metal resistance Rch2, measured from Kelvin structures and with metal Rtot2 which is from direct measurements with the metal routing.

There are both N-type and P-type MOSFET transistors; 6V, 30V, 120V, 150V and 200V operation voltages; total channel widths equal to 10K μm or 20μm. All the detailed data are listed in Table Ⅰ. Ideally, the resistances of 10K μm devices are 2 times to those of 20K μm devices. However, Rm1 of 10K μm device is not equal to 2 times to that of 20K μm device. This is because the high voltage devices (> 100V) are with race-track type layouts, not rectangle layouts. Hence, the metal routing in high voltage devices is not the metal in parallel. Furthermore, Rch2 of 6V NMOS transistor with channel width equal to 20K μm (6V_N_20K) becomes smaller than 0.1Ω so it cannot be obtained at the typical machine.

TABLE I
MOSFET Resistances on SOI

Device Name	Channel Rch1 (Sim.)(Ω)	Interconnect Rm1 (Sim.)(Ω)	w/o metal Rch2 (Meas.) (Ω)	with metal Rtot2 (Meas.) (Ω)
6V_P_10K	0.7090	0.0377	0.7210	0.7520
30V_P_10K	2.9495	0.0304	3.0862	3.1129
150V_P_10K	15.5900	0.0297	14.8898	14.9151
6V_P_20K	0.3545	0.01846	0.3590	0.3720
30V_P_20K	1.4747	0.0152	1.5410	1.5410
150V_P_20K	7.7952	0.0381	7.4230	7.4230
6V_N_10K	0.1785	0.0371	0.1790	0.2040
30V_N_10K	0.8430	0.0317	0.8560	0.8730
120V_N_10K	3.9940	0.0260	3.9410	3.9620
150V_N_10K	4.8044	0.0287	4.6380	4.6700
200V_N_10K	6.9510	0.0273	6.6500	6.6900
6V_N_20K	0.0892	0.0178	<0.1	0.1010
30V_N_20K	0.4210	0.0163	0.4180	0.4340
120V_N_20K	1.9970	0.0358	1.9300	1.9600
150V_N_20K	2.4020	0.0305	2.3000	2.3400
200V_N_20K	3.4759	0.0440	3.3490	3.3900

Red data: resistances don't fit the device sizes, namely R@10K≠(R@20K)*2.

There are three equations as follows:

(1) Metal ratio= Rm1/ Rch1

(2) Simulation (Sim.) ratio= Rtot2/ (Rch1+Rm1)

(3) Spice ratio= Rtot2/ Rch1

The small Sim. ratio or Spice ratio indicates that real layout areas will not be increased a lot so the ratio should be as small as possible. As the device operation voltage is increased, the channel resistance Rch1 is increased. Therefore, the metal ratio will be decreased no matter in 10K μm or 20K μm devices. In Fig. 1, both Sim. ratio and Spice ratio data are illustrated. Spice ratio follows the trend of Metal ratio (not shown in the picture). Its value is from 95% to 115%. It demonstrates 15% extra layout area should be added from Spice simulation. However, Sim. ratio is from 95 % to 105% so only 5% extra layout area should be added.

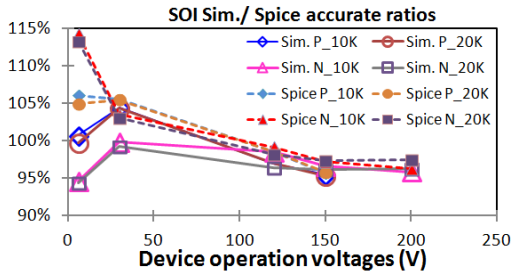

Fig. 1. Sim./Spice accuracies vs. Device operation voltages in SOI platform

III. BCD Data Results and Analyses

The data similar to SOI are exhibited in BCD-1 platform, but there are much more devices so BCD-1 raw data are not listed. Rch1 in BCD is from 0.2 Ω to 3.5 Ω and Rm1 is from 0.04 Ω to 0.08Ω. Sim. ratio equal to 90%~ 110% and Spice ratio equal to 95%~120% can be seen in Fig. 2. In small voltage devices, Rm1/ Rch1 is big so Spice ratio becomes big. Spice data don't include metal data so a big metal ratio (not shown in the figure) resulted in a big Spice ratio.

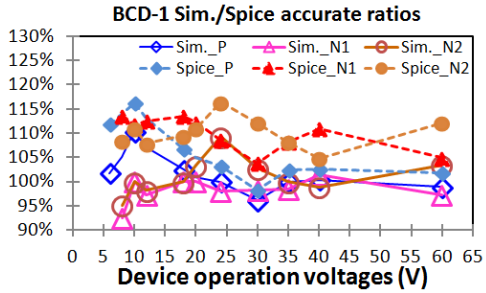

Fig. 2. Sim./Spice accuracies vs. Device operation voltages in BCD-1 platform

In BCD-2 platform, huge LAD is discovered and data are listed in Table Ⅱ. Fig. 3 demonstrates Sim. ratio equal to 95%~100% and Spice ratio equal to 105%~130%.

TABLE Ⅱ
MOSFET Resistances on BCD-2 platforms

Device Name	Channel Rch1 (Sim.)	Interconnect Rm1 (Sim.)	w/o metal Rch2 (Meas.)	with metal Rtot2 (Meas.)
6V_P_77.5K	0.0918	0.0276	0.0918	0.1155
12V_P_60K	0.2928	0.0288	0.2928	0.3184
6V_N_26.5K	0.0695	0.0170	0.0695	0.0840
18V_N_24K	0.1390	0.0212	0.1390	0.1564
30V_N_31K	0.1534	0.0293	0.1534	0.1809
12V_N_10K	0.2746	0.1478	0.3108	0.4351
12V_N_23K	0.1455	0.0186	0.1455	0.1625
12V_N_50K	0.0546	0.0530	X	0.0939
12V_N_50K_CUP	0.0545	0.0336	X	0.0636
12V_N_100K	0.0273	0.0470	X	0.0597

50K μm devices and 100K μm devices are for real productions so there are no Kelvin structures for w/o metal measurements.

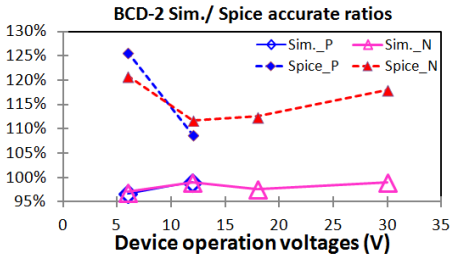

Fig. 3. Sim./Spice accuracies vs. Device operation voltages in BCD-2 platform (12V data are with 23K μ m.)

In Fig.4, from the device width concerns, Metal ratio and Spice ratio are with the same trend. Except 12V_N_10K, Spice ratio increases as the channel width increases because of high metal ratio at large channel width devices. In 10K μm, the metal routing is with top metal connections, but for other size devices, they are used by Metal-3 and top metal as the major connections so 12V_N_10K is excluded in the trend.

Except 12V_N_50K_CUP, Spice ratio can reach 110%~220%, but Sim. ratio can be kept in 80%~105%. For

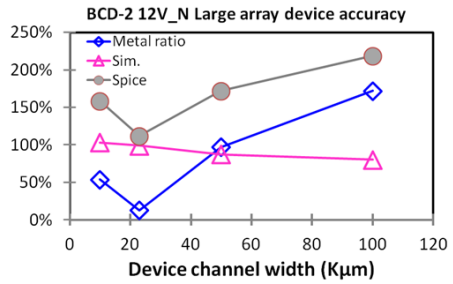

Fig. 4. Sim./Spice accuracies vs. Device operation voltages in BCD-2 platform

Circuit Under PAD (CUP), R3D evaluates the resistance layer by layer, but real IC has current flowing vertically entering the devices so the real product has a much lower resistance.

IV. Design Flow Modifications

If IC driving capability can be over driven, we can reach IC driving target by amplifying the channel width in 1.1 times to the simulation size. If the new design flow can be adopted, such as Fig. 5, the layout size can be reduced about 40%. Then, the consumer electronic IC will become more competitive.

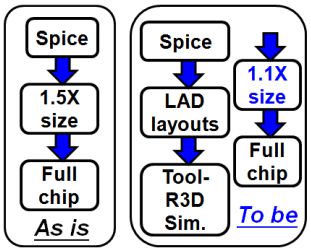

Fig. 5. A new proposed IC design flow

V. Conclusions

In this study, one new consumer electronic IC design flow is proposed. Just use the simple tool for evaluating LAD driving capabilities. Then, IC will become more cost saving.

References

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