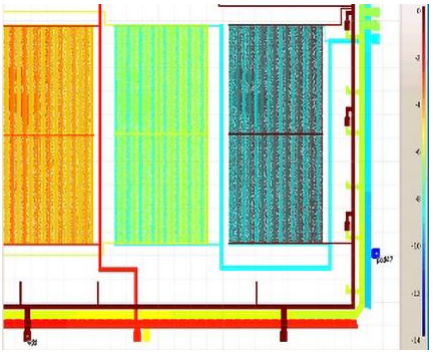
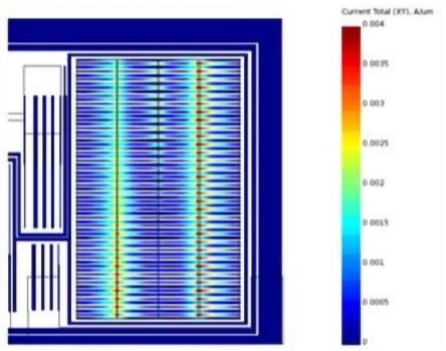
DATASHEET

ESRA

Full-Chip ESD Verification, Analysis and Sign-off

ESD devices protect sensitive circuits from electrical discharges but the complex circuit topology of today's designs make ESD protection difficult. A detailed understanding of the current flow and potential distributions in the ESD protection circuit is essential to optimize the device layouts and to ensure a balanced current distribution, low resistance, and efficient connection to power nets. Traditional parasitic extraction and simulation tools are inadequate to describe these effects.





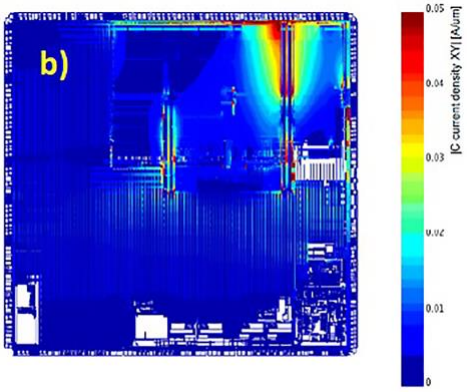
ESRA (Electrostatic Reliability Analysis) is a full-chip ESD analysis solution. It identifies weak points in ESD protection circuit and supports ESD sign-off for both HBM and CDM standards. ESRA delivers extraction, analysis, and debugging capability in one integrated environment with the capacity to analyze the full chip. Highlighted violations permit engineers to perform corrections at any time in the design process.

ESRA is built on production-proven technologies from Silicon Frontline, including fast and guaranteed accurate parasitic extraction and circuit-proven, high-capacity matrix solvers. It includes layout-based, full-chip visualization and debugging of current density and potential distribution, and is seamlessly integrated within existing design flows.

ESRA supports the latest technologies and is validated with silicon measurement. With ESRA, engineers can identify ESD protection failures in their design before tape-out and prevent in-field failures.

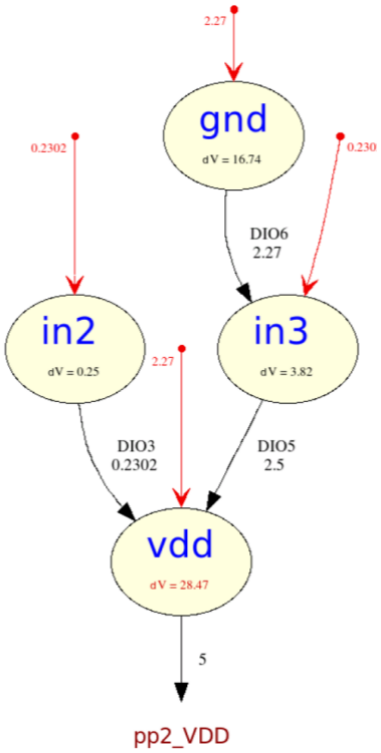
FEATURES

- Full-chip ESD verification and analysis
- Proven on leading technology (5nm full-chip design)
- Unlimited capacity, over 15B transistors
- The only full-chip solution for both HBM and CDM
- Verifies device, interconnect and package
- Supports inductance and transient effects
- Seamless integration with existing post-layout verification flow
- Ease of use visualization and debugging



Comprehensive ESD Analysis

ESRA replaces manual ESD checks with automated verification of ESD protection networks for electrical connectivity, resistance, and current density checks. ESRA quickly identifies issues in the layout and analyzes weak elements of ESD network. A detailed simulation and analysis of ESD protection devices and network elements ensures efficiency of electrical connections and their compliance with current density and resistance rules.

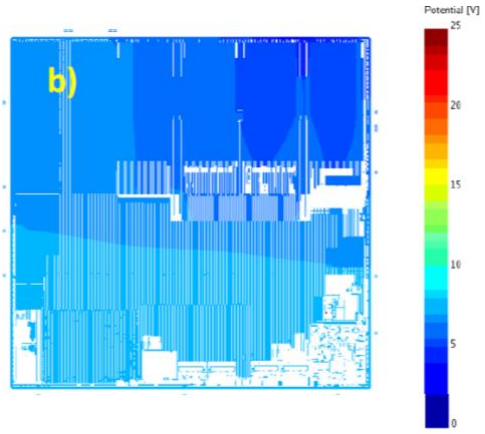


ESRA performs both HBM and CDM ESD reliability analysis at IP and full-chip level. It analyzes several failure types such as:

- Gate oxide overstress
- PN junction overstress
- Current density overstress
- ESD device overstress
- Capacitor or inductance connected to MOS gates
- Excessive resistance

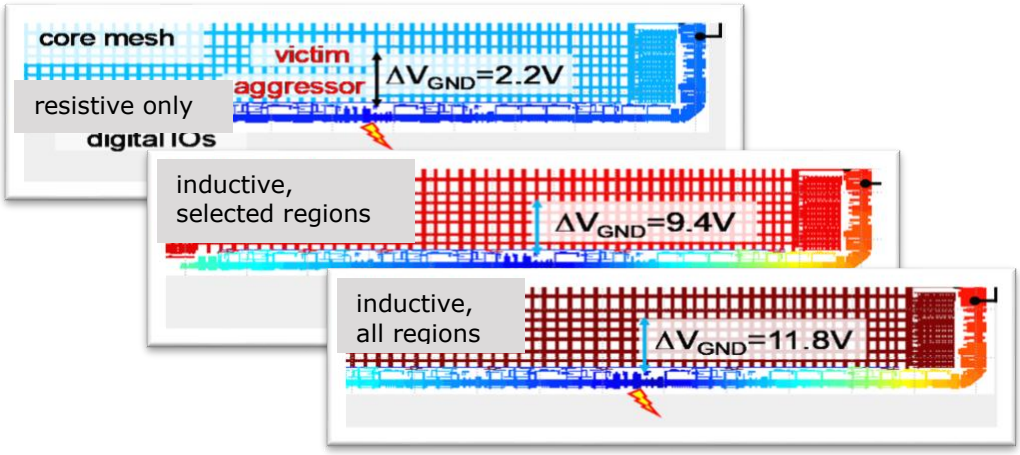
Accurate IP and Full-chip ESD Analysis

Ensuring simulation of accurate discharge path requires correct identification of ESD devices. ESRA employs pattern matching to automatically identify all ESD devices and locates the exact position of these devices in the full-chip design.

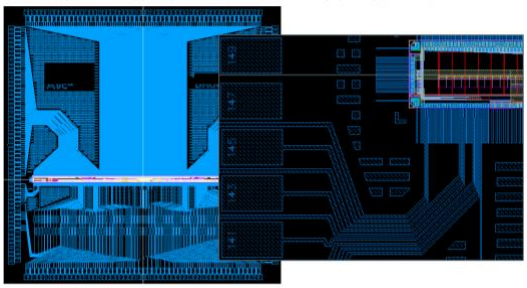


Both internal ESD and non-ESD devices are susceptible to failure during an ESD event. ESRA's stress checking feature reports device location, severity of stress violation, and provides visualization of current flow through ESD and non-ESD devices. It supports different stress limits based on HBM or CDM modeling.

Inductance of long metal lines can have significant impact on the accuracy of ESD simulation. ESRA automatically accounts for both bus and package inductance during ESD simulation. By scanning the database and extracting the inductance, it detects critical areas of the design and provide silicon accurate current distribution and potential hot spot detection.

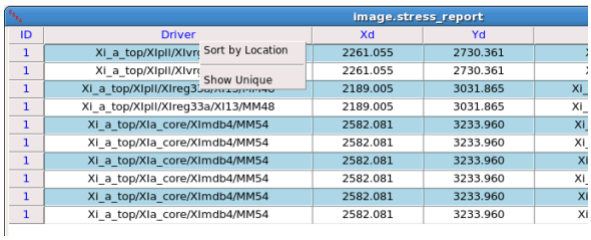


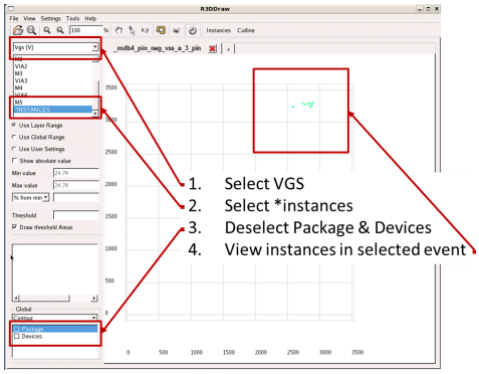
Running ESD verification early in the design stage allows ample time to identify issues and make any required structural changes prior to full-chip sign-off. However, an incomplete layout presents issues when trying to perform a true ESD analysis on IP blocks. ESRA block-level CDM flow allows ESD analysis with a partial top-level layout by virtually connecting supply and ground locations of the IP with package pins.

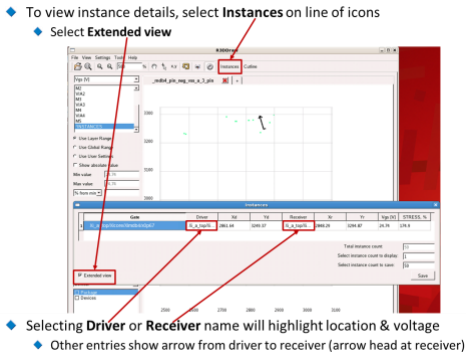


Seamless Integration and Ease-of-Use

ESRA integrates with existing back-end flows and supports GDS and CCI layout inputs. It's hierarchical debugging offers telescopic and microscopic views of the design for faster debug. ESRA GUI-based visualization environment annotates overvoltage to layout highlighting problems related to excessive resistance, current density, and voltage drops.







ESRA from Silicon Frontline

ESRA ensures that ESD design guidelines are met by highlighting weak areas of the design, pinpointing susceptible devices and providing reports of current density violations and high resistance paths. With ESRA, engineers gain greater confidence in the reliability of their design, achieve first time design success, and avoid costly design revisions.

CONTACT

Silicon Frontline Technology, Inc.
4030 Moorpark Avenue, Suite 249
San Jose CA 95117
408-963-6916
info@siliconfrontline.com
www.siliconfrontline.com