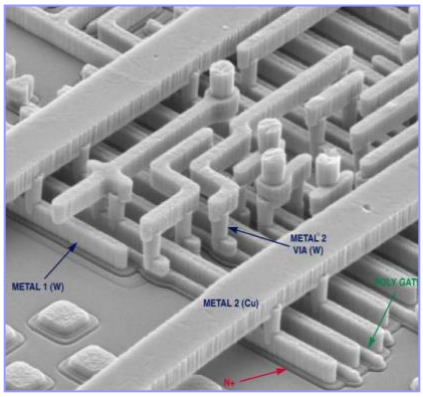
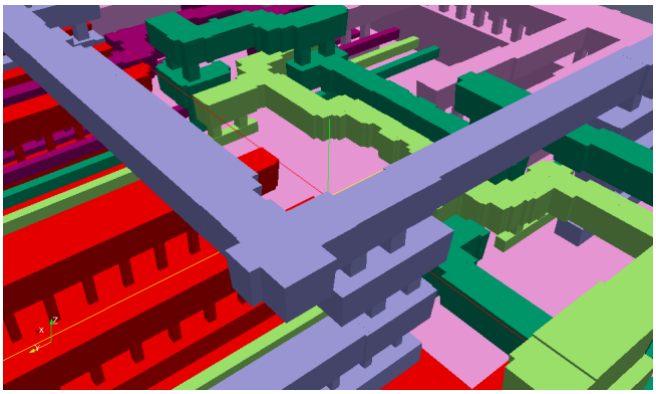
DATASHEET

PILLAR

Fast Layout Analysis and Debug

Designers know that parasitic devices can impact a chip's functionality and performance. Unexpected parasitic devices can throw off the balance of differential signals and parasitic bottlenecks can have a catastrophic impact on high performance or timing sensitive nets. Debugging parasitic devices is often a lengthy and incomplete process involving script generated spreadsheets and cumbersome manual interaction with layout. Parasitic bottlenecks are hidden in millions of parasitic elements and can be located anywhere on the chip. It is like finding a needle in the haystack. What designers need is a fast, easy to learn, and complete layout analysis and debug tool.

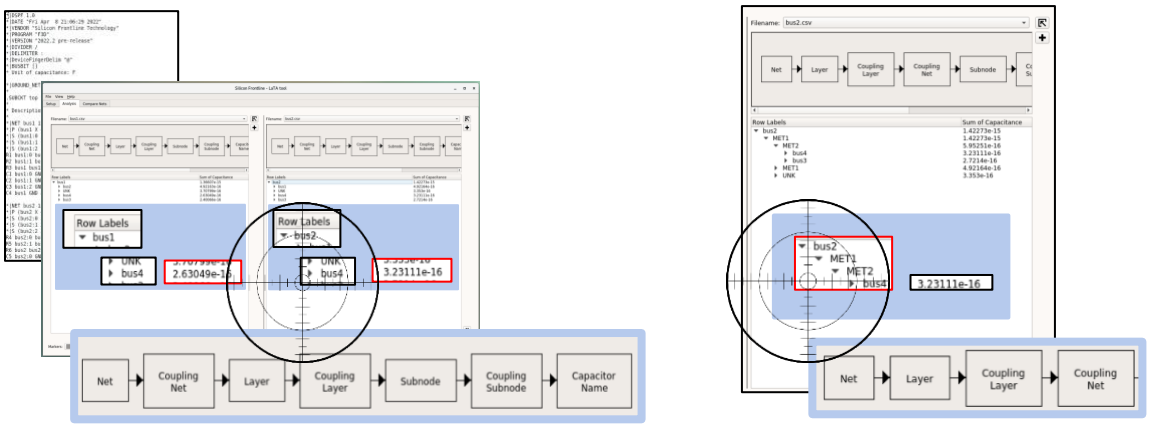




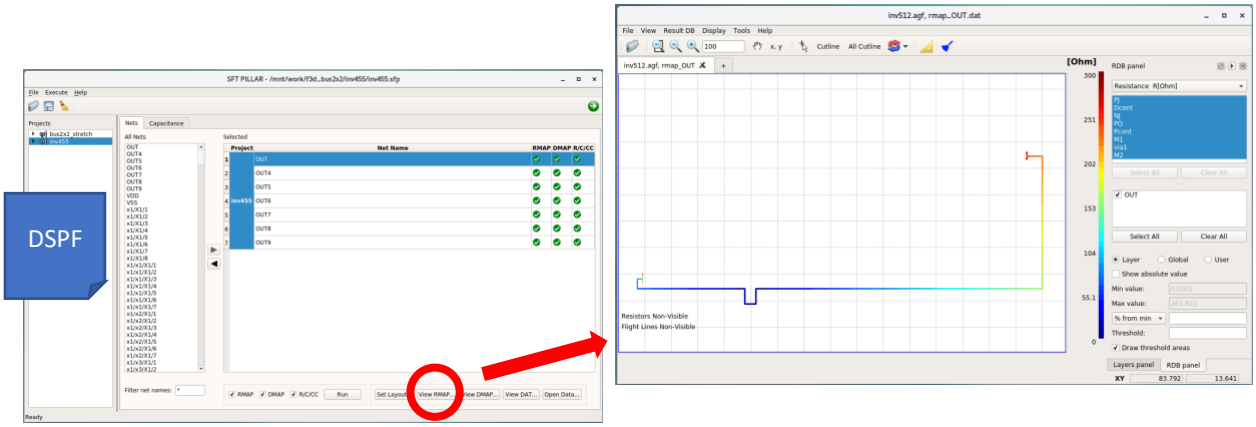
PILLAR adds power to manual flows by allowing designers to see, find and fix their parasitic problem fast. It integrates into standard flows and provides a complete intuitive environment with exhaustive visualization filtering. By leveraging the designer's knowledge, PILLAR provides actionable data to fix their layout.

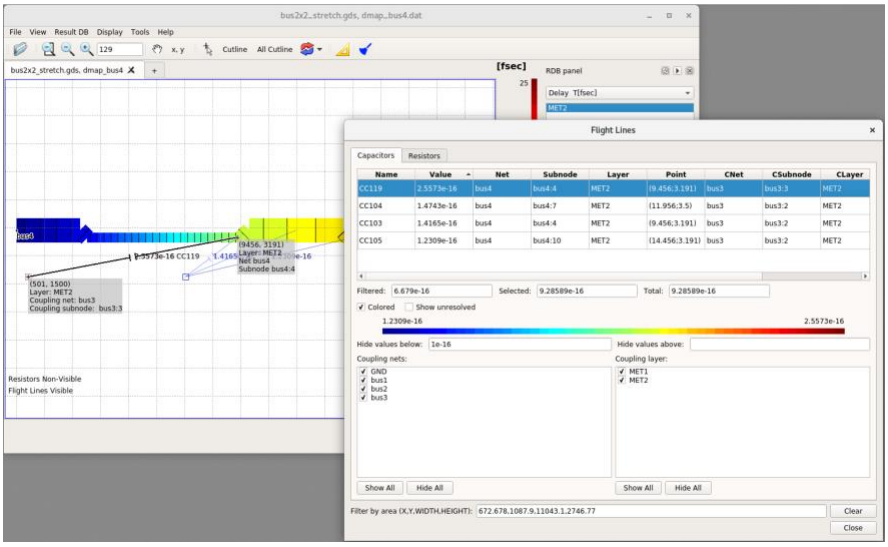
Intuitive Interactive Debugging

PILLAR reads in DSPF directly and helps designers to quickly see anomalies in their layout. Designers can manipulate hierarchical pivots to find issues in coupling nets or identify metal layers that are causing the problem.



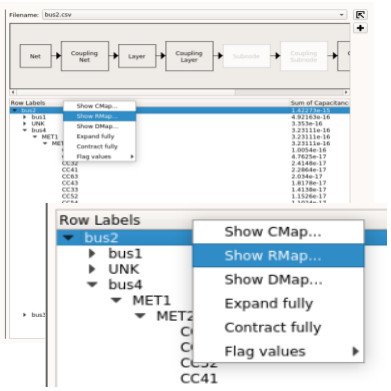
With PILLAR, designers can see point to point resistance, find the resistors involved in bottlenecks and the layers they reside in, and formulate a fix. It also provides a simple way to see how timing propagates along the nets, interactively probe the delays, and gain insight into where the bottlenecks exist.

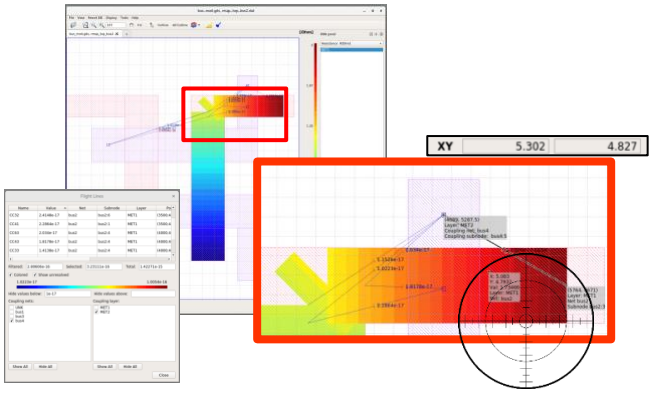




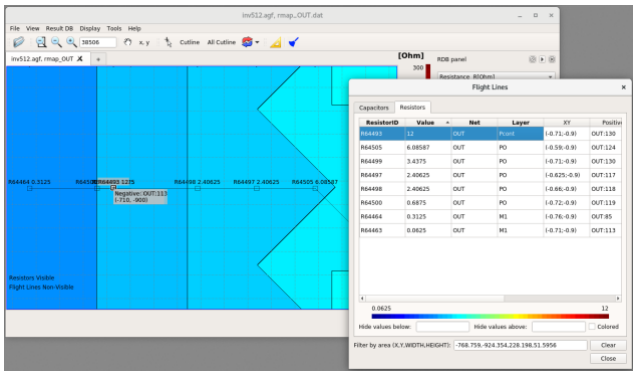
Exhaustive Visualization Filtering

Designers can visualize DSPF with PILLAR industry-leading data and layout viewer and quickly identify a problem by viewing capacitance, resistor, or delay maps. Exhaustive visualization filtering allows designers to filter the layout by net, by layer, and minimum or maximum capacitance, then color them to help identify the problem.

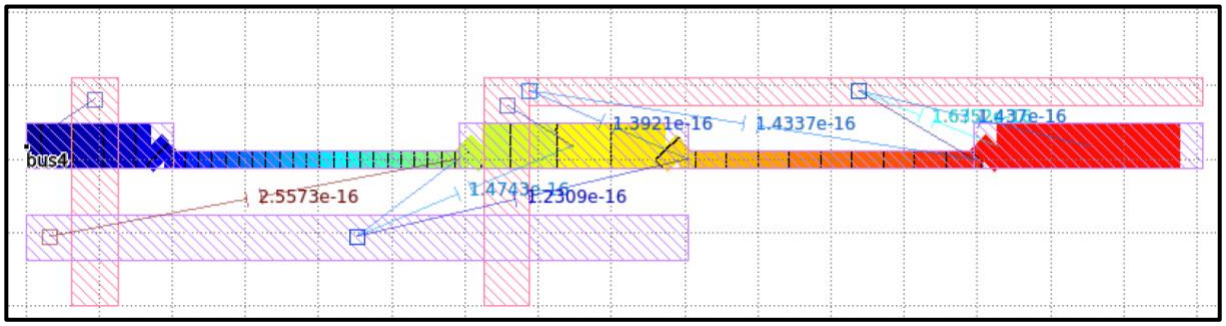




With the visualization capabilities of PILLAR, designers can annotate resistance slope to help locate areas for deeper analysis and identify where high rates of resistance changes exist. Slope annotation of coupling capacitance can highlight nets and layers involved in delay bottlenecks.

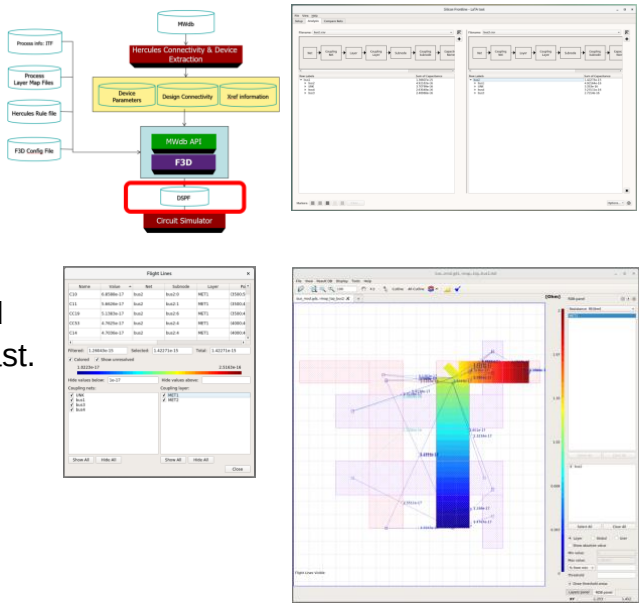


Augmenting the data over the layout allows designers to create actionable information and easily fix their issue.



See, Find, and Fix Parasitic Problems Fast

PILLAR adds power to manual layout debug. It is a fast layout debug and analysis solution with industry leading viewer and exhaustive visualization filtering. Designers can leverage their design knowledge to quickly **See** anomalies due to parasitic problems; **Find** parasitic devices augmented on layout; and armed with this information **Fix** problems fast.



CONTACT

Silicon Frontline Technology, Inc.
4030 Moorpark Avenue, Suite 249
San Jose CA 95117
408-963-6916
info@siliconfrontline.com
www.siliconfrontline.com